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USAAVSCOM TR 92-D-4



US ARMY AVIATION
AND TROOP COMMAND

SMART INTEGRATED MICROSENSOR SYSTEM (SIMS)

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November 1992

Final Report

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Prepared for

AVIATION APPLIED TECHNOLOGY DIRECTORATE
US ARMY AVIATION AND TROOP COMMAND
FORT EUSTIS, VA 23604-5577

93-00574

43 pcf

92 1 02 026

AVIATION APPLIED TECHNOLOGY DIRECTORATE POSITION STATEMENT

This report presents the design and development of a prototype Smart Integrated Microsensor System (SIMS) module designed to measure the cyclic strain loading exerted on a helicopter component and calculate an estimate of lift degradation caused by that strain. Since fatigue damage cannot be seen, fatigue critical components are currently replaced when they reach a set operating time limitation. This limitation is based on the projected use of the helicopter fleet. The SIMS module described in this report enables the replacement of these parts based on actual damage accumulated. Thus, the SIMS has the potential of increasing flight safety while simultaneously reducing maintenance downtime and parts usage.

Mr. Paul Redden of the Reliability, Maintainability and Mission Technology Division served as project engineer for this effort.

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1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE November 1992	3. REPORT TYPE AND DATES COVERED Final October 1987 - February 1992	
4. TITLE AND SUBTITLE Smart Integrated Microsensor System (SIMS)			5. FUNDING NUMBERS (C) DAAJ02-89-C-0038	
6. AUTHOR(S) Mel Fujita				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) ELDEC Corporation Monitor and Control Division 13700 13th Avenue W. Lynnwood, WA 98045			8. PERFORMING ORGANIZATION REPORT NUMBER 011-4920-203 Rev. A	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) Aviation Applied Technology Directorate U.S. Army Aviation and Troop Command Fort Eustis, VA 23604-5577			10. SPONSORING/MONITORING AGENCY REPORT NUMBER USAAVSCOM TR 92-D-4	
11. SUPPLEMENTARY NOTES				
12a. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution is unlimited.			12b. DISTRIBUTION CODE	
13. ABSTRACT (Maximum 200 words) This report details the design and development of the Smart Integrated Microsensor System (SIMS). SIMS is a sensor that measures fatigue in materials and components and displays it in an easy-to-understand readout.				
14. SUBJECT TERMS Microsensor Integrated Microsensor Fatigue Life			15. NUMBER OF PAGES 37	
			16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT UNCLASSIFIED	18. SECURITY CLASSIFICATION OF THIS PAGE UNCLASSIFIED	19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED	20. LIMITATION OF ABSTRACT	

PREFACE

This report presents the technical description of the SIMS (Smart Integrated Microsensor System) design. It also summarizes the major activities of the program with recommendations for the future development of the SIMS concept.

The ELDEC Corporation would like to thank the Aviation Applied Technology Directorate (AATD) for the cooperation and support in achieving this important element in the evolution of the SIMS concept. Our special thanks go to Paul Redden and Randy Buckner of AATD.

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INTRODUCTION

The current method of replacing components based on operating hours must assume a projected usage and take into account uncertainties in the actual usage by increasing the loads or modifying the S-N curves, or both. This provides a clearly inefficient part replacement criteria. It is still possible for a component to see more severe usage than originally anticipated, and cause a component to fail before the operating time limit has expired. It is very likely that most components will not see the loading originally predicted. Since the nature of fatigue is such that damage increases exponentially with load, these components will therefore be replaced long before they need to be. Many may be replaced with little or no damage accumulated at all. Since there is no way of inspecting for damage short of destroying the part, the parts must be discarded. A significant amount of maintenance downtime is spent replacing these parts. The SIMS design (see Figure 1) concept provides a more accurate knowledge of the fatigue damage than current techniques. This knowledge is presented to the maintainer in a clear, easy-to-understand read-out of the real-time percentage of fatigue life remaining. This will increase overall system safety and reduce both parts usage and maintenance downtime.



FIGURE 1. SIMS MODULE.

With the advent of microelectronics (e.g. ASIC) and new stress/strain analysis techniques, a microelectronics system that monitors, analyzes and displays the remaining fatigue life in real-time would provide an optimal means of attaining good life data and maximize the performance life of the helicopter. This system entails the utilization of state-of-the-art ASIC (Application Sensitive Integrated Circuit) and other SMT (Surface Mount Technology) devices; along with implementation of fatigue life algorithms such as Palmgren-Miner Damage rule and a simple rainflow counting in microelectronics devices.

Numerous studies have been conducted in the area of real-time fatigue life prediction methods, but there has been limited success in implementation.

1.1 PROGRAM OBJECTIVE/PURPOSE

The program objective was to develop a stand-alone Smart Integrated Microsensor System (SIMS) for real-time measurement of fatigue life of high-failure-rate materials on Army Helicopters such as the swashplate (7049-T73 aluminum) on the AH-64. A device of this nature would provide an immediate means of assessing component remaining fatigue life

The purpose of the program was to design and build a set of units to validate the technique of real-time fatigue measurement in a small self-contained battery-powered microelectronics package.

1.2 DESIGN DEVELOPMENT APPROACH

The basic design approach was to combine the fatigue analysis algorithms proven through helicopter experience by the Army with the ELDEC experience in microcircuitry design to develop the SIMS module.

1.3 SIMS DEVELOPMENT OVERVIEW

The SIMS development started with a review of the concept of using an ASIC implementation of the Miner's rule algorithm, but it became apparent the concept would not provide the necessary sampling rate (continuous) to capture all the stress/strain cycles for an accurate measure of fatigue life. There were additional tradeoff studies to consider the best combination of:

- Size, weight and cost
- Reliability and maintainability
- Sampling rate
- Resolution
- Calibration
- Environmental Durability

1.4 SUMMARY

A total of three modules were assembled and delivered to AATD with a design documentation package. Two configurations were developed so the units could be tested on different materials.

The first two were configured to measure fatigue stress of 7049-T73 aluminum. These units were shipped to AATD on 21 January 1992.

The third unit was shipped on 4 February 1992. It was calibrated for 4340 alloy Steel.

The design represents only a "Proof of Concept" configuration. Further miniaturization for production versions is feasible and can be accomplished on future configurations.

1.5 SYSTEM OVERVIEW DESCRIPTION

1.5.1 General

The components of the SIMS system are as follows:

1. SIMS MODULE

The SIMS module is a solid-state electronic device that receives stress/strain signals from a specified material via a strain gage. The strain gage signals are signal conditioned and converted to digital data. The data is then processed through an algorithm that detects the stress/strain cycles and calculates the cumulative fatigue damage on the material in real-time based on the material S/N curve (per MIL-HDBK-5E). The fatigue life is displayed as the percent of remaining life on an electrochemical indicator. There is also an IR serial port to transmit the fatigue data to an external display device.

The module is a composition of microelectronics devices housed in a 1 x 3.12 x 4 inch case. The SIMS overall functionality breaks down into the following elements:

- Instrumentation amplifier and filter
- A/D converter
- Peak detection logic
- Rainflow fatigue algorithm logic
- Curve fitting logic
- Data display interfaces

The SIMS module system diagram is shown in Figure 2.

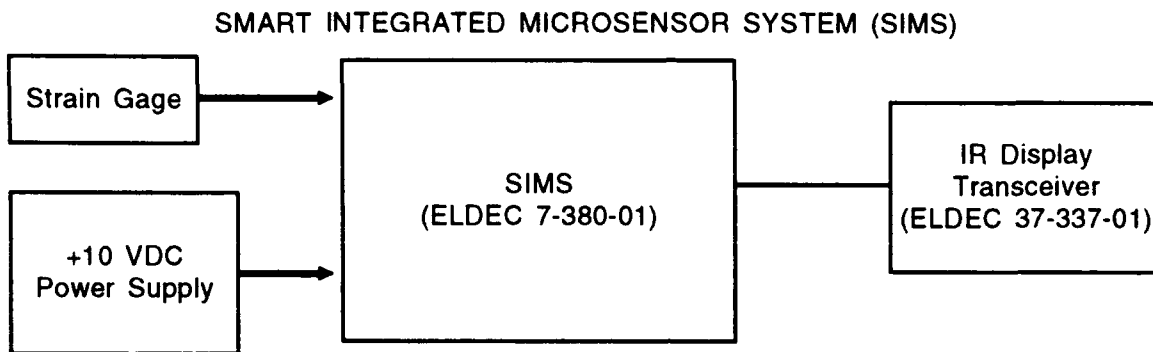


FIGURE 2. SYSTEM DIAGRAM.

2. STRAIN GAGE (CFE)

The strain gage (customer furnished) is mounted on the specific material of either 7049-T73 aluminum or 4340 alloy steel. Other materials can be used; however, the module will require modification/recalibration. The recommended strain gage is an EA-series type (Micro-Measurements Inc.), but equivalent types can be used.

3. INPUT POWER SOURCE (CFE)

The input power for the SIMS module is $+10\text{Vdc} \pm 0.1 \text{ Vdc}$ with 200 mA capacity. The power requirement consists of 95 mA steady state, 150 mA transient condition. The power is divided between the module electronics and the electrochemical display.

Module Electronics = 35mA

Electrochemical Display = 60mA

4. IR REMOTE DISPLAY (CFE)

The IR (Infrared) Remote Display is an electronic IR transmitter/receiver display unit that reads fatigue data from the IR port on the SIMS module and displays it on a set (8) of 7 segment LEDs. This is a specialized piece of test equipment designed for the SIMS module application.

The display consists of a IR Wand, interconnect cable and display unit. The IR Remote Display is available from ELDEC (part number 37-337-01).

1.5.2 SIMS System Description

The strain gage signal is conditioned by a instrumentation amplifier (part of U11) which amplifies the signal and filters (LP) it for noise. The amplified/filtered signal is then converted to digital form through a 5-bit A/D converter (U11). A digitized peak detector (U2) samples the A/D data when the conversion is complete and determines whether or not a peak (maximum) or a valley (minimum) has occurred. When such an event occurs, the corresponding peak or valley is stored until a "matching" valley or peak is received. The "matched pair" constitutes a "closed cycle." The rainflow fatigue algorithm logic and the summation algorithm counts the "closed" cycles and correlates them to the material S/N curve implemented in U3,U4. When stress cycles are closed the relative magnitude of the cycle is sent to the curve fitting logic (U5) and a corresponding fatigue count is generated. These fatigue counts are accumulated in a 24-bit register.

The fatigue count data (closed cycles) can be read on a IR port (U1, D1) or displayed on the Remaining Life Display (U9) as percent of remaining fatigue life. See Figure 3.

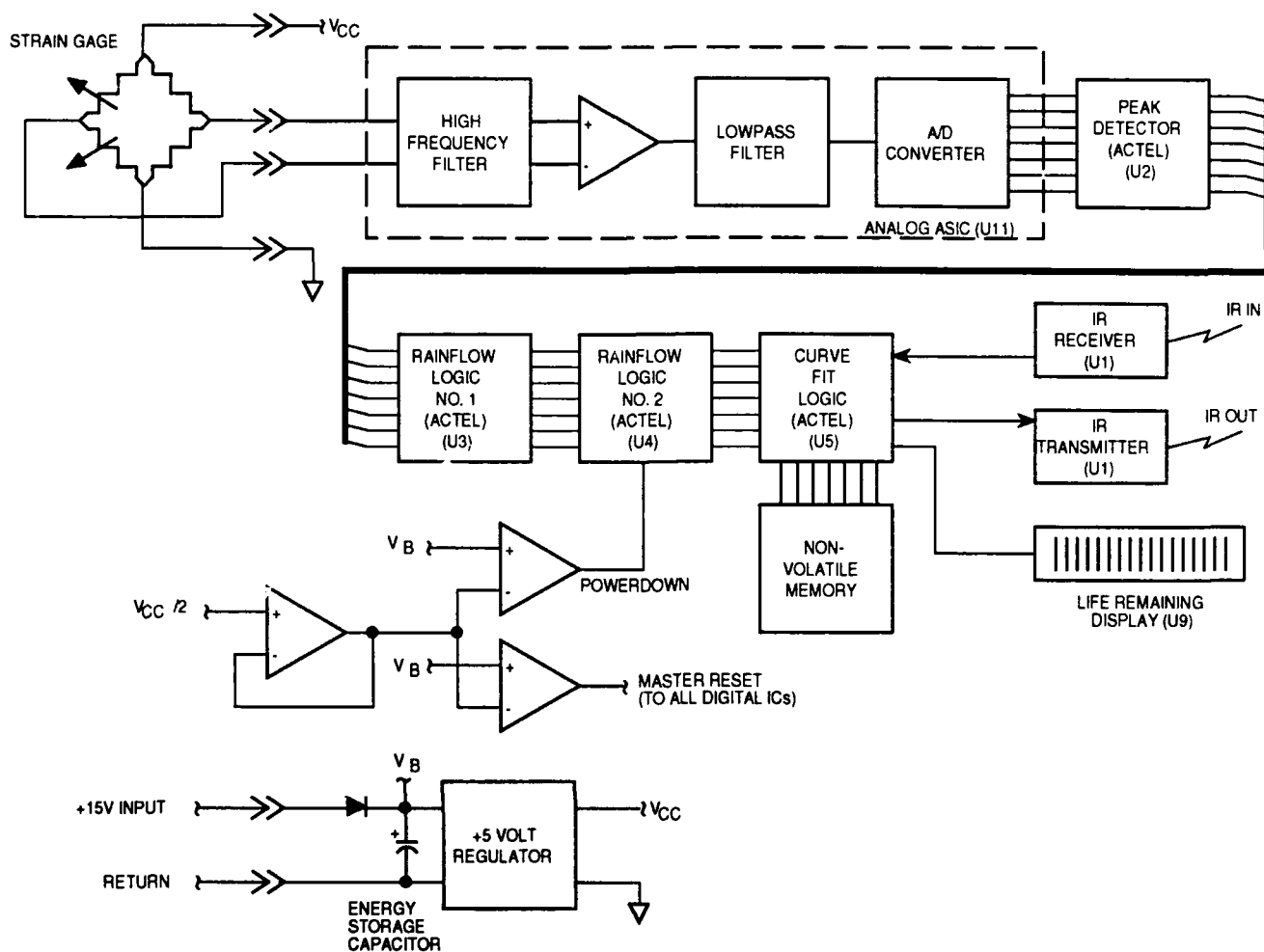


FIGURE 3. SIMS FUNCTIONAL BLOCK DIAGRAM.

1.5.3 ASIC Design

The ASIC for the SIMS design was developed using a Plessey CMOS mixed mode array (MH array series). With these arrays all devices (transistors, resistors, capacitors, etc.) are preprocessed with fixed locations, some being optimized for analog and some for digital. The user only modifies one step in the process, the metal interconnect that connects the devices together to create the circuit. The advantage of this approach is low cost and quick prototypes, both of which were important to the SIMS design given its experimental nature and budget limitations. CMOS was chosen because it is the best current technology for combining low power analog with digital circuitry on the same IC.

One of the challenges of the design was the front end amplification since the signal from the strain gage is relatively low (200mv); therefore, extra effort was applied to ensure low noise in the sense amplifier as well as provide manual offset adjust.

Although the array approach was clearly the most appropriate for this phase of the design, a full custom approach would allow integration of the ASIC and Actel chips into only one ASIC and reduce the power to microwatts instead of milliwatts.

1.5.4 Real-Time Fatigue Life Algorithm Development

The development of a real-time process for measurement/calculation of fatigue life damage involved research into a number of technical papers on the subject. The study revealed an article by S.D. Downing and D.F. Socie published in January 1982 on application of techniques in fatigue life predictions. Specifically, the article described a technique of using the RAINFLOW algorithm which allowed real-time stress/strain cycle measurements that gave identical results as the standard method of having the entire load history before the cycle counting process starts. This advantage of real-time cycle counting is the basis for the "on-board" processing developed for the SIMS module.

The Downing/Socie real-time random load analysis algorithm is referred to herein as RAINFLOW cycle. This algorithm is regarded as the best means of obtaining a real-time prediction of fatigue life by pairing high maxima with low minima data.

The RAINFLOW stress/strain cycles are summed into a damage accumulation, or fatigue life data, using a summation formula called MINERS RULE. This rule, along with the material S-N curve, provide a fairly accurate measurement of a given material's remaining fatigue life.

These algorithms were implemented in Field Programmable Array Modules (4) as "Hard Logic." The modules are manufactured by ACTEL and are CMOS Technology containing 2,000 programmable logic gates. Each module is a 68-pin surface mount device.

The digital logic section of the SIMS module contains four ACTEL devices and a RAM. Programmed in these devices are the peak detector, rainflow algorithm, sequencing control, and curve fitting logic.

The peak detector device contains logic functions for the 5-bit SAR A/D converter and a peak detection algorithm. The peak detector is designed to detect peaks and valleys for the rainflow algorithm. This is accomplished through the use of flip-flops to store states and digital comparators of previous values.

The rainflow logic is designed to reproduce the rainflow algorithm as described in the Downing and Socie paper. The device consists of three main sections: RAM pointers, computation logic, and control logic. There are three RAM pointers that are used to read and write data as the algorithm is processed in real time. The S-register holds a starting reference location. The Y-register points to where the Y data range is located. The DP, or data pointer, indicates how many data values are stored in RAM. The computation logic consists of registers, comparators, adders, and subtractors, all of which are used for the processing of the data per the rainflow algorithm. The control logic contains RAM control and rainflow control logic. This control logic serves as the core of the rainflow algorithm implementation.

The sequencing control device contains logic functions for the IR link, power-up control, and power-down control. The IR link control consists of a 34-bit register and control logic to output the proper sync pattern and data. The power-up and power-down control sections initialize the other devices and contain the logic necessary to retain the counts and pointers in the RAM when power is no longer available.

The curve fitting logic device contains a data table, multiplier, and a fatigue count register. The data table is pre-programmed with a given set of multipliers. The fatigue register is a 24-bit register that contains the total number of fatigue counts. This register is stored and recalled during power-down and power-up respectively.

The overview of the operation is as follows:

1. The peak detector determines a peak or valley and notifies the rainflow algorithm device.
2. The rainflow algorithm device (Actel) stores the value in RAM and creates X and Y ranges based on the rainflow algorithm. The X and Y ranges are then processed with the computation logic. If the result is to count the Y range, then the Y range value is sent to the curve fitting device.
3. This range is weighted according to its magnitude by multiplying it by one of the values from the data table (S-N curve). The result is a fatigue count (based on a maximum of 16.7 million) that gets added to the current overall fatigue count. The result is a running total of a percentage of life left in a given material.

A. Display

Remaining fatigue life is an output of the Curve Fit Logic (CFL) ACTEL and is reflected on an electrochemical column indicator, which is a nonvolatile display.

B. IR Transceiver

This is a secondary data port for verifying the remaining fatigue life. The IR Receiver (input LED) receives a CLOCK INPUT strobe from the IR Link Remote Display test equipment (ELDEC P/N 37-337-01). The module then shifts data out of the IR transmitter (output LED) synchronous with the input clock.

1.5.5 Packaging Design

Although the module packaging was in the spirit of a production design, it is based on the electronic design that uses developmental parts rather than production style. Therefore the size and weight is greater than a production unit. Since the module has more mass distributed over wider spans, the fundamental resonance is lower. The unit will survive reasonable shipping and handling loads, but is not as robust as a smaller, lighter production version would be.

The assembly was designed to allow easy access to the circuit card (7-380600-01). Each of the covers (7-380201-01, 7-380202-01) can be removed separately for access to either side of the circuit card assembly.

The circuit card assembly (7-380600-01) is a stand-alone electrically functional unit. Pins (4) are mounted in the corners of the card to prevent rotation of the covers during assembly/disassembly.

The circuit card assembly contains 80 percent SMT components and is soldered and assembled to ELDEC workmanship standards. The card is conformal coated (polyurethane).

The circuit card is clamped around its edges on both sides by the covers and attached to the covers at the center. The card acts as a diaphragm supported around the edge and supported in the center.

The length of the shoulder on the spacer (7-380203-01) and the length of the nut (7-380204-01) have been selected to ensure that there will be a gap between these parts and the captive screw retainers in the covers. Tightening the cover mounting screws pulls the centers of the covers toward the circuit card and prestresses the covers.

The covers provide structural integrity, a Faraday cage for some degree of EMI/RFI protection, and a physical barrier to prevent shorting and damage to the circuit card.

The covers also function as structural base for some methods of mounting the unit. However, the design of the module focused on ease of access and packaging of the prototype electronics, rather than as a demonstration of mounting techniques.

The spacer and the nut were designed to work with commercially available cover mounting hardware while using the least amount of board area.

The nut (on the bottom side of the card) secures the spacer to the circuit card. The spacer provides the internal threads for both the top and bottom covers. Loads on one cover will react with the spacer and the other cover. The spacer will keep the motion of the centers of the covers in phase.

Any tendency of the center of the card to move toward the bottom cover will load the spacer in tension. These are the only loads (other than assembly pre-load) that will be applied to the nut and to the external threads on the spacer.

Any tendency of the center of the card to move toward the top cover will load the spacer in compression.

These parts only need sufficient pre-load to ensure that they will both remain in contact with the card. The parts are bonded to each other with an anaerobic sealant to ensure that they will remain attached to the card when the covers are removed.

The nameplate (7-380205-01) provides identification of the unit by model and serial number. Each circuit card is programmed for a particular material S-N curve and identified by serial number. Therefore it is important to make sure serial number on the card and cover are the same.

Since it is very easy to swap covers between units, tracking serial numbers are stamped on the circuit card. The serial number on the nameplate is a convenience and the user is responsible for ensuring that the proper cover is installed on the assembly. This will be easy to check since the card serial number will be the same as the number on the nameplate and the serial number will be visible from the top of the circuit card.

1.5.6

Environmental Performance

A. Temperature

The limiting factor on temperature is the threshold that the electronic components will survive. These components are cooled by radiant and natural convection (to transfer energy to the covers). The covers can then transfer heat to the atmosphere by radiation and natural convection.

Since the mercury column display will not normally operate at the low temperature extremes, a heater (PTC) is provided. Heat is provided as an inverse function of the ambient temperature; therefore, the heater will not waste energy in warmer environments. This solution has been proven in breadboard tests of the unit.

Some relative motion will occur between the covers and the circuit card due to the different coefficients of thermal expansion.

The pre-load on the installed covers will ensure that the edges of the covers will remain in contact with the card at low temperatures.

B. Temperature Shock

The maximum rate of change of temperature is limited by the ability of the surface mount parts to stay attached to the card. Our experience has shown that these parts will survive temperature shock of 10 °C per minute.

C. Vibration

The prototype units are capable of surviving random vibration from 2 to 2,000 Hz at 10g. The first resonance will be over 500 Hz.

D. Humidity

The circuit card assembly is solder-masked and conformal coated.

The connector is moisture sealed. It uses a silicone elastomer compression interfacial seal to provide a moisture and humidity seal between each contact and between the contacts and the connector shell.

Therefore the unit can be stored or operated at 95% humidity.

E. EMI

The SIMS module is not considered to contain any significant radiated emission risks due to:

Operating frequency is 1 MHz or lower.

Power level is 950 mW or less.

Circuit Card is multilayer with internal ground planes.

Additional grounding points have been added to the unit if needed.

EMI tests have not been performed.

F. Mounting Requirements

The case provides a flat surface on the top and bottom that can be mounted with adhesive.

The unit can be strapped in place, clamped, mounted with Velcro fasteners, or bonded with adhesive.

The base of the unit can also provide a means for bolting the unit directly to a surface.

The base of the unit is 3.12 x 4.00 inches. The connector comes out on one of the short sides. A one inch square area must be kept clear around the connector to allow for attaching the mating connector.

1.5.7 Electrical Interface

The connector is mounted on the side of the case. The cable can be routed in any direction to avoid interference.

The connector is a Micro-D metal shell PCB mount with socket contacts. The ITT Cannon part number is MDM-9SCBRP.

An example of a mating part is:

ITT Cannon part number MDM-9PSLA30

SIMS MODULE DETAIL DESIGN

This section describes the mechanical and electrical components used in the design. Also included is an outline of performance tests conducted during acceptance/development tests.

2.1 MODULE COMPONENT LISTING

There are a total of 142 parts (8 mechanical and 134 electrical) in the SIMS module.

2.1.1 Mechanical Components

The eight mechanical piece parts are:

<u>PART TITLE</u>	<u>PART NUMBER</u>	<u>QTY</u>
1. Cover, Top	7-380201	1
2. Cover, Bottom	7-380202	1
3. Spacer	7-380203	1
4. Nut	7-380204	1
5. Nameplate	7-380205	1
6. Screw	PEM PS10 832	2
7. Circuit Card	7-380600	1
		<hr/>
		TOTAL 8

The 7-380-01 "Top Assembly" (see Figure 4) shows how the mechanical pieces are assembled. The following subsections describe how each part is fabricated. All parts are controlled by ELDEC drawings.

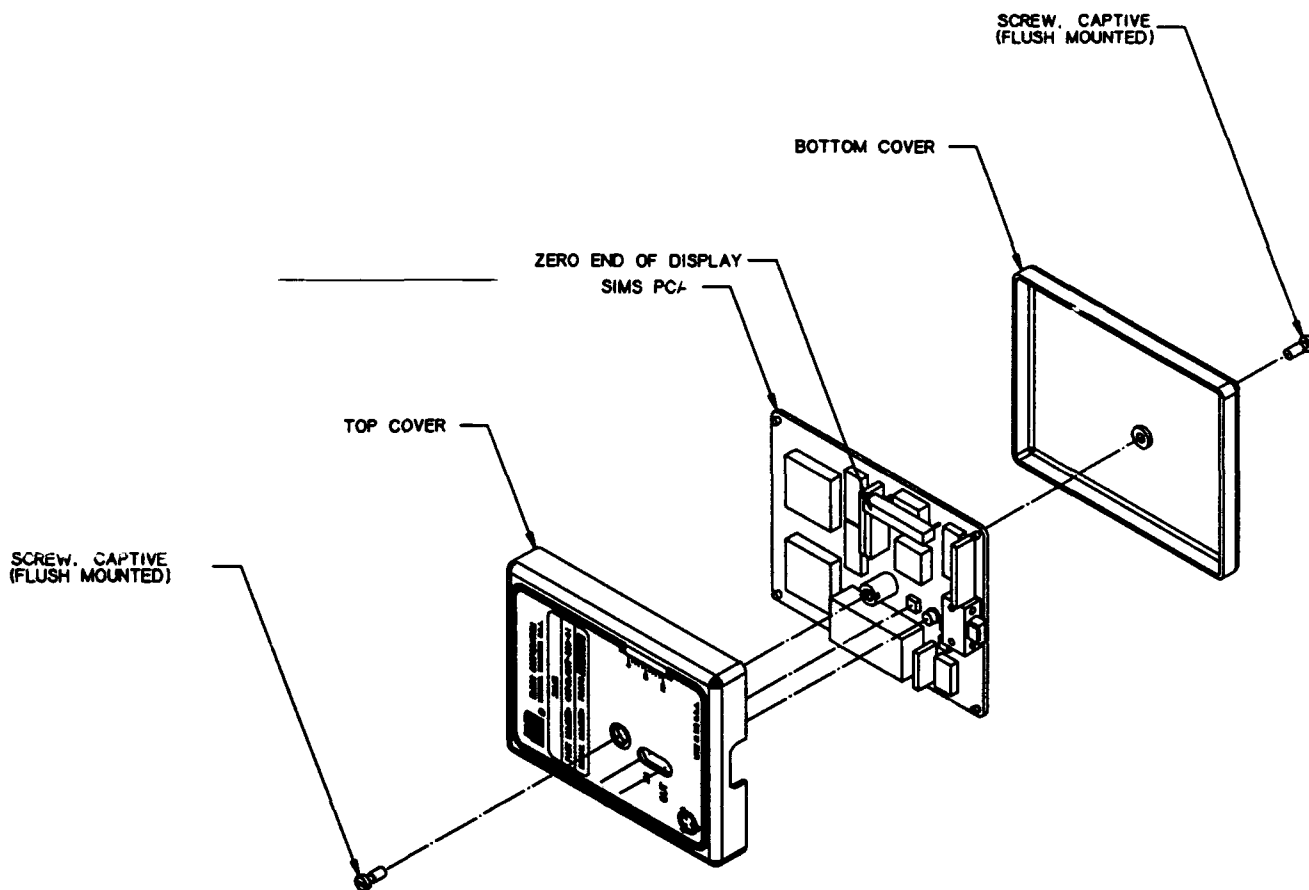


FIGURE 4. TOP ASSEMBLY VIEW.

2.1.1.1 Top Cover (7-380201-01)

The top cover is made from a deep-drawn aluminum can (Zero Corporation part number ZT50-64B-9). The nominal wall thickness is 0.06 inch. The details are machined at ELDEC per ELDEC workmanship standards. The finished part is painted. The cover has one opening in the wall that is for the external connector. The cover has three top openings. A rectangular hole is for access to the IR transmitter and the IR receiver. A rectangular opening is provided for viewing the "life remaining" display. The third hole has a flush-mount captive screw retainer (PEM part number PR10 832) pressed in place. The cover is painted black.

2.1.1.2 Bottom Cover (7-380202-01)

The bottom cover is made from a deep-drawn aluminum can (Zero Corporation part number ZT50-64B-6). The nominal wall thickness is 0.06 inch. The details are machined at ELDEC per ELDEC workmanship standards. The cover has a flush-mount captive screw retainer (PEM part number PR10 832) pressed in place. The bottom is painted black.

2.1.1.3 Spacer (7-380203-01)

The spacer is stainless steel. Its internal threads accept the captive screws from the covers. The top portion provides a shoulder that rests against the top side of the circuit card. The bottom portion provides external threads that pass through the circuit card and accept the nut (7-380204-01). A slot in the top end of the spacer provides a means for applying torque.

2.1.1.4 Nut (7-380204-01)

The nut is stainless steel. The internal threads mate with the external threads of the spacer. The body rests against the bottom side of the circuit card. A slot in the bottom end of the nut provides a means for applying torque.

2.1.1.5 Nameplate (7-380205-01)

The nameplate is made from 0.02 inch-thick, black image, photosensitive aluminum foil. Film adhesive, which can be activated by heat or solvent, is used to attach the nameplate to the top cover. The nameplate identifies the unit by name (SIMS), manufacturer (ELDEC Cage Number 08748), ELDEC part number (7-380-01), serial number and a label identifying the material to which the unit is calibrated.

2.1.1.6 Screws (PEM PS10 832)

The screws that hold the covers onto the circuit card assembly are commercial hardware (PEM part number PS10 832 40). These screws are captive in retainers that are pressed into the covers. The screws are flush to the covers when the covers are installed.

2.1.1.7 Circuit Card Assembly (7-380600-01)

The circuit card assembly is the heart of the system. It contains all the electronics to receive the strain gage inputs, process the data and display the measured fatigue life in real-time. It consists of an 8-layer, 3.8 x 2.9 x 0.063 inch printed circuit board (FR4 material) with 134 components mounted on both sides of the board.

2.1.2 Electrical Components

There are a total quantity of 134 electrical and electronic parts (22 different types). This subsection describes each part type, function and quantity. All of these components are located on the circuit card assembly. Figure 5 is a layout of all the components and their location.

The following is a list of the PART TYPE/NUMBER/QTY:

<u>PART TITLE</u>	<u>PART NUMBER</u>	<u>QTY</u>
Capacitor	CWR06K.....	3
Capacitor	CDR32B.....	4
Capacitor	CDR33B.....	1
Diode	CR96-01	1
Infrared	LEDMF0E1102	1
Programmable Switches	AD-ESD...L	4
PWB	7-380601-01	1
Pos. Temp. Coefficient Resistor	21091	1
Connector (9 pin)	MDM-9SCBR	1
Field Effect Transistor	IRFD110	1
Resistor (SMD)	RE67-01XXXX.....	33
Resistor Networks	MSP0XX-01.....	4
Terminal Strip(Test Points)	TSW-1-12-07-L-S	68
IR Receiver	ULN-3360T	1
Field Programmable Gate Array	ACT 1020-PL68I	4
Nonvolatile SRAM (16k)	DS1220AB-150-IND	1
Comparator	CMP04FS	1
Miniature Elapsed Time Meter	620PC-2	1
Linear Regulator	MAX663ESA	1
Hex Inverter	74HCU04	1
ASIC	7-380801....	1
PNP TRANSISTOR	2N2222A	1
TOTAL		134

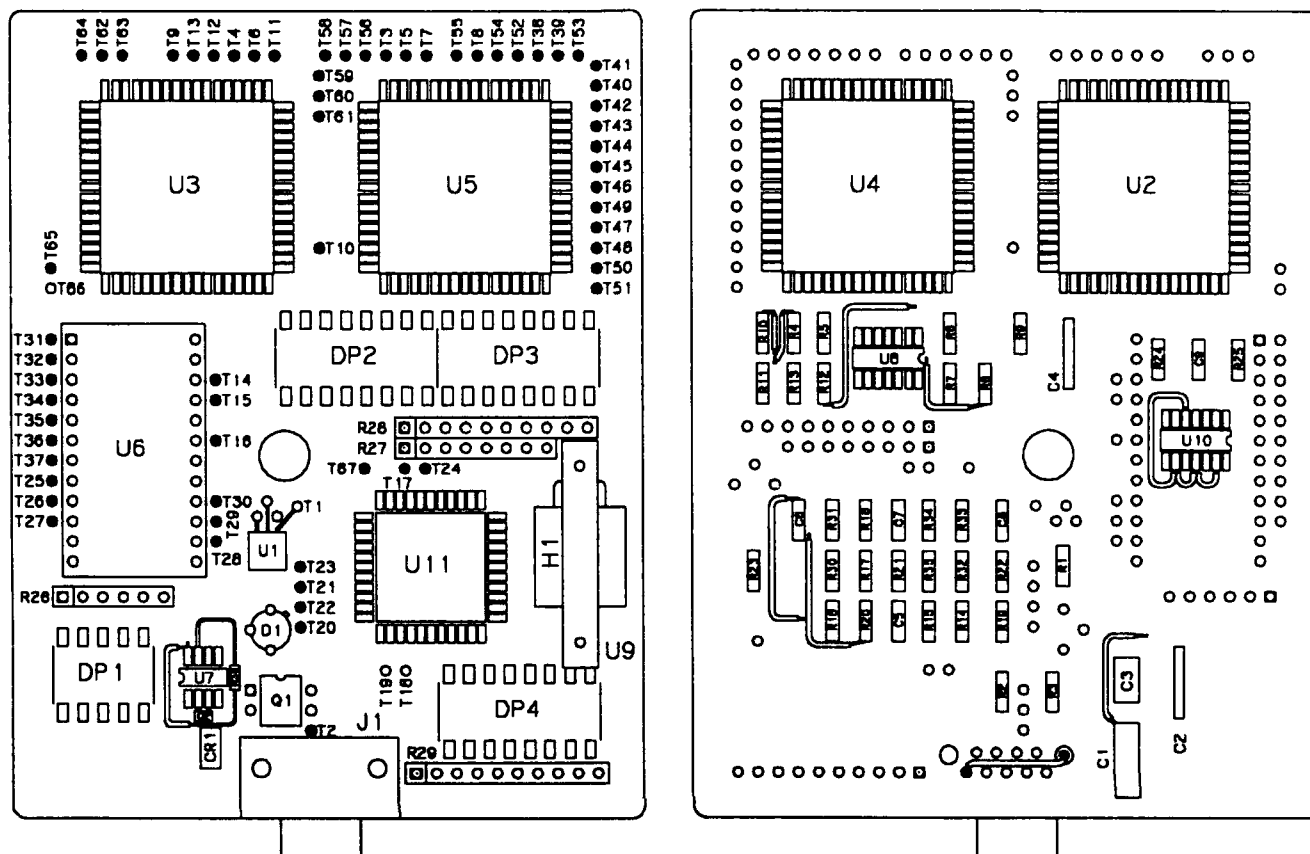


FIGURE 5. COMPONENT LAYOUT AND LOCATIONS.

2.1.2.1 Capacitor: CWR06KAXXXKR

A. PART DESCRIPTION:

This is a tantalum fixed chip capacitor per MIL-C-55365. It is encapsulated porous tantalum with an oxide semiconductor electrolyte. It is used for surface mount applications and has a voltage rating of 25.

B. FUNCTION:

The capacitors (three) are used as:

1. Storage capacitor (C1) used on the input regulator.
2. Filter capacitors (C2, C4) for Vcc and the Power Up/Down Sequence.

C. SOURCE: Multiple

2.1.2.2 Capacitor: CDR32BPXXXBKUM

A. PART DESCRIPTION:

This is a fixed, multiple-layer ceramic chip capacitor per MIL-C-55681/8. The ceramic dielectric has better temperature stability than other types of capacitors.

B. FUNCTION:

This capacitor (C5,6,7) is used for filter networks on the strain gage input amplifiers (ASIC). It is also used as a timing capacitor (C9) on the system clock.

C. SOURCES: Multiple

2.1.2.3 Capacitor: CDR33BX104AKUM

A. PART DESCRIPTION:

This is a fixed, multiple-layer ceramic chip capacitor per MIL-C-55681/8. The ceramic dielectric has better temperature stability than other types of capacitors.

B. FUNCTION:

This capacitor (C3) is used for filter on the output of the +5Vdc regulator.

C. SOURCES: Multiple

2.1.2.4 Diode: CR96-01

A. PART DESCRIPTION:

This is a chip-style silicon switching diode that is equivalent to the 1N4150 series diodes under MIL-S-19500.

B. FUNCTION:

This diode (CR1) is used as a blocking diode for the +10Vdc input.

C. SOURCES: Unitrode, Microsemi

2.1.2.5 Infrared LED: MF0E1102

A. PART DESCRIPTION:

This part (D1) is a fiber-optic infrared LED device. It is used in fiber-optic application due to its high-power (5 mW) and medium frequency response (up to 10 MHz). It is hermetically sealed in a TO-5 style package.

B. FUNCTION:

The LED is the transmitter for the IR port. It is mounted to allow transmission through a hole in the top cover.

C. SOURCES: Motorola

2.1.2.6 Programmable Switches: AD-ESDXXXL

A. PART DESCRIPTION:

These are surface-mount DIP style switches. The switches come in forms containing 2 to 10 positions. The contact resistance is 50 mΩ over an industrial temperature range.

B. FUNCTION:

The SIMS module circuit card uses two styles:

1. Eight-position switch (Qty 3):

One (DP4) is used for ASIC Zero Adjust; two (DP2, DP3) are used for the curve fitting coefficients.

2. Five-position switch (Qty 1):

This switch (DP1) is used for the RAINFLOW mode select and MEMORY RESET.

C. SOURCES: Assmann Electronics

2.1.2.7 Printed Wiring Board (PWB) 7-380601-01

This is the bare circuit board designed and built by ELDEC. It is a custom designed board only for this application. It is 3.8 inches x 2.9 inches x 0.063 inch. The PWB is eight layers thick and made of epoxy (FR4) glass laminate. The trace width, pad sizes, and spacing are per IPC Std 782. The layout requires components on both sides of the board. The board density is 80%, which allows for some expansion. Also, there are 68 test points which are for the prototype only.

A. FUNCTION:

The PWB is the circuit board for all the electronic/electrical components.

B. SOURCES: ELDEC Corp.

2.1.2.8 Positive Temp. Coefficient (PTC) Resistor 21091

A. PART DESCRIPTION:

This resistor (H1) changes its resistance as a function of temperature. It contains a flame-retardant polymer.

B. FUNCTION:

The PTC is used as a "heater blanket" for the display that is sensitive to "cold temperatures." As the temperature decreases the PTC heats up, thereby keeping the display warm. The reverse occurs as the temperature rises.

C. SOURCES: Raychem

2.1.2.9 Connector (nine pin) MDM-9SCBR

A. PART DESCRIPTION:

This is a MICRO-D connector selected for its size and pin count (nine pins).

B. FUNCTION:

The connector (J1) is the electrical interface for input power (+10 Vdc) and strain gage inputs.

C. SOURCE: ITT Cannon

2.1.2.10 Field Effect Transistor IRFD110

A. PART DESCRIPTION:

This is a 1-Watt N-Channel MOSFET transistor in a four-pin DIP package. It uses HEXFET technology that provides low resistance while maintaining most of the MOSFET features.

B. FUNCTION:

This MOSFET (Q1) is used as the drive source for the IR transmitter (see 2.1.2.5).

C. SOURCE: International Rectifier

2.1.2.11 Resistor (SMD) RE67-01XXXX

A. PART DESCRIPTION:

This is a surface mount, thick-film resistor. It is a 1206 style that offers 1% and 0.125W over a full military temperature range.

B. FUNCTION:

These resistors (RX) of various values are used primarily on the ASIC strain gage amplifiers as well as the linear regulator/power up/down circuit.

C. SOURCES: Allen Bradley, Dale, MEPCO

2.1.2.12 Resistor Networks MSP0XA-01

A. PART DESCRIPTION:

These are SIP (Single-In-Line) 1k resistor networks. Networks come in 5, 7 or 9 resistor packages and each is connected between a common pin and PC board pin.

B. FUNCTION:

These SIPs (R26,27,28,29) are used as 1k ohm "pull-ups" for the programmable switches (see 3.1.2.5).

C. SOURCE: Dale

2.1.2.13 Terminal Strip (Test Points) TSW-1-12-07-L-S

A. PART DESCRIPTION:

This is a strip of 12 terminals. Each terminal is a 0.025 square post, 0.230 long. They are individually soldered into the circuit card as a test point via PTH (Plated Thru Hole). There are a total of 68 test points.

B. FUNCTION:

These terminals (68) serve as test points for the inputs/outputs of the four ACTEL modules and the ASIC. The test points are only to assist in the SIMS module checkout. They serve only as monitor points and have no operational value.

C. SOURCE: SAMTEC

2.1.2.14 IR Receiver ULN-3360T

A. PART DESCRIPTION:

This is an opto-electronic switch integrated with an amplifier, comparator, power driver and a regulator. Its input is a photodiode with operation up to 30 kHz.

B. FUNCTION:

This IC (U1) is the receiver for the IR port. It is located next to the IR transmitter.

C. SOURCE: Allegro Micro

2.1.2.15 Field Programmable Gate Array (FPGA) ACT 1020-PL68I

A. PART DESCRIPTION:

The FPGA is the heart of the SIMS module. It is a CMOS device that employs ACTEL's antifuse technology to program the device. The ACTEL 1020 contains 2,000 logic gates that are nonvolatile and permanently programmable. A system performance of 40 MHz is possible.

B. FUNCTION:

Four of the FPGAs are used in the SIMS module. Two (U3,4) are used to implement the RAINFLOW algorithm, one (U2) is for the PEAK DETECTOR, and the last (U5) is for the CFL (Curve Fitting Logic). The ACTEL is packaged in a 68 pin LCC (leadless chip carrier). Each ACTEL chip is soldered directly to the circuit board.

C. SOURCE: ACTEL

2.1.2.16 Nonvolatile SRAM (16k) DS1220AB-150-IND

A. PART DESCRIPTION:

The nonvolatile SRAM is a 16k-bit fully static, nonvolatile RAM with a self-contained lithium battery energy source and control circuitry to switch to battery power when Vcc is in an out-of-tolerance condition. The memory uses CMOS technology with 150 ns access times. It is packaged in a standard 28-pin JEDEC case.

B. FUNCTION:

The SRAM (U6) is the storage location for the "UNCLOSED CYCLES" that might exist during a power shutdown. Data will be stored in the SRAM when it detects a loss of power. It makes data available when Vcc is restored. The expected RAM utilization is 1k. The SRAM has a data retention life of up to 10 years.

C. SOURCE: Dallas Semiconductor

2.1.2.17 Quad Comparator CMP04FS

A. PART DESCRIPTION:

The comparator is a low-power precision 14-pin SO narrow body surface mount device. It has a low input offset of 1mV (max) with the capability of using a single supply (+5 Vdc).

B. FUNCTION:

The comparator (U8) is used for the POWER-UP/DOWN shutdown circuit.

C. SOURCE: PMI

2.1.2.18 Miniaturemil Elapsed Time Meter 620PC-2

A. PART DESCRIPTION:

The elapsed time meter is a CURTIS microcolumnar (two columns of mercury separated by an electrolyte gap). As current is passed through the tube it causes mercury to electroplate from the ANODE to CATHODE. The gap location is proportional to the current-time integral.

B. FUNCTION:

The meter (U9) is used as a display device for the REMAINING FATIGUE LIFE. It is pulsed by the output of the CFL module (ACTEL) and scaled to the "FULL LIFE" of the material.

C. SOURCE: CURTIS Instruments

2.1.2.19 Linear Regulator MAX663ESA

A. PART DESCRIPTION:

The MAX663 regulator is a CMOS voltage regulator with a dual mode (+5V or adjustable) capability. It has an output capacity of 40 mA. The regulator package is an 8-pin gull-wing surface mount.

B. FUNCTION:

This regulator (U7) provides the +5 Vdc for all the SIMS electronics. The input voltage is +10 Vdc and power required is approximately 100 mW.

C. SOURCE: MAXIM

2.1.2.20 Hex Inverter 74HCU04

A. PART DESCRIPTION:

The Hex Inverter is a standard CMOS logic device. The "HCU" style has low gain characteristics that are suitable for this specific application. The package is a Small Outline Integrated Circuit (SOIC).

B. FUNCTION:

This Hex Inverter (U10) was selected for its low gain characteristic that is necessary for a clean square wave system clock oscillator.

C. SOURCE: Motorola

2.1.2.21 ASIC 7-380801

A. PART DESCRIPTION:

The ASIC is a custom design developed by ELDEC for specific application to the SIMS module. It has been designed to provide specific amplifiers for the strain gage input, 200 kHz filter and A/D converter. It is packaged in a 44-pin LCC.

B. FUNCTION:

The ASIC (U11) provides specific operational amplifier for the SIMS module.

C. SOURCE: ELDEC Corp.

2.1.2.22 NPN Transistor 2N2222A

A. PART DESCRIPTION:

The NPN transistor is a standard low power silicon bipolar transistor. The package is an SOIC.

B. FUNCTION:

This transistor (Q2) is used as a booster for the +5Vdc regulator that will provide additional capacity if necessary.

C. SOURCE: ELDEC (TR128-01), Motorola, National

2.2 SYSTEM PERFORMANCE VERIFICATION

2.2.1 Test Equipment

The equipment used to perform the system performance tests is similar to that used for the breadboard tests. The following is the list of test equipment:

<u>ITEM</u>	<u>EXAMPLE</u>
Waveform Generator	WaveTek Model 148A *
Logic Analyzer	Phillips PM 3585
IR Remote Display Tester	ELDEC 37-337-01
Digital Sampling Oscilloscope	Tektronix Model 2430
386PC with DAC Board	Everex *
Power Supplies	
+10Vdc :	Kikusui PAB32-2A
+2.5Vdc:	Kikusui PAB32-2A *
	(Offset)
Test Cable	ELDEC

* For strain gage simulation only, see Figure 6 for typical test setup.

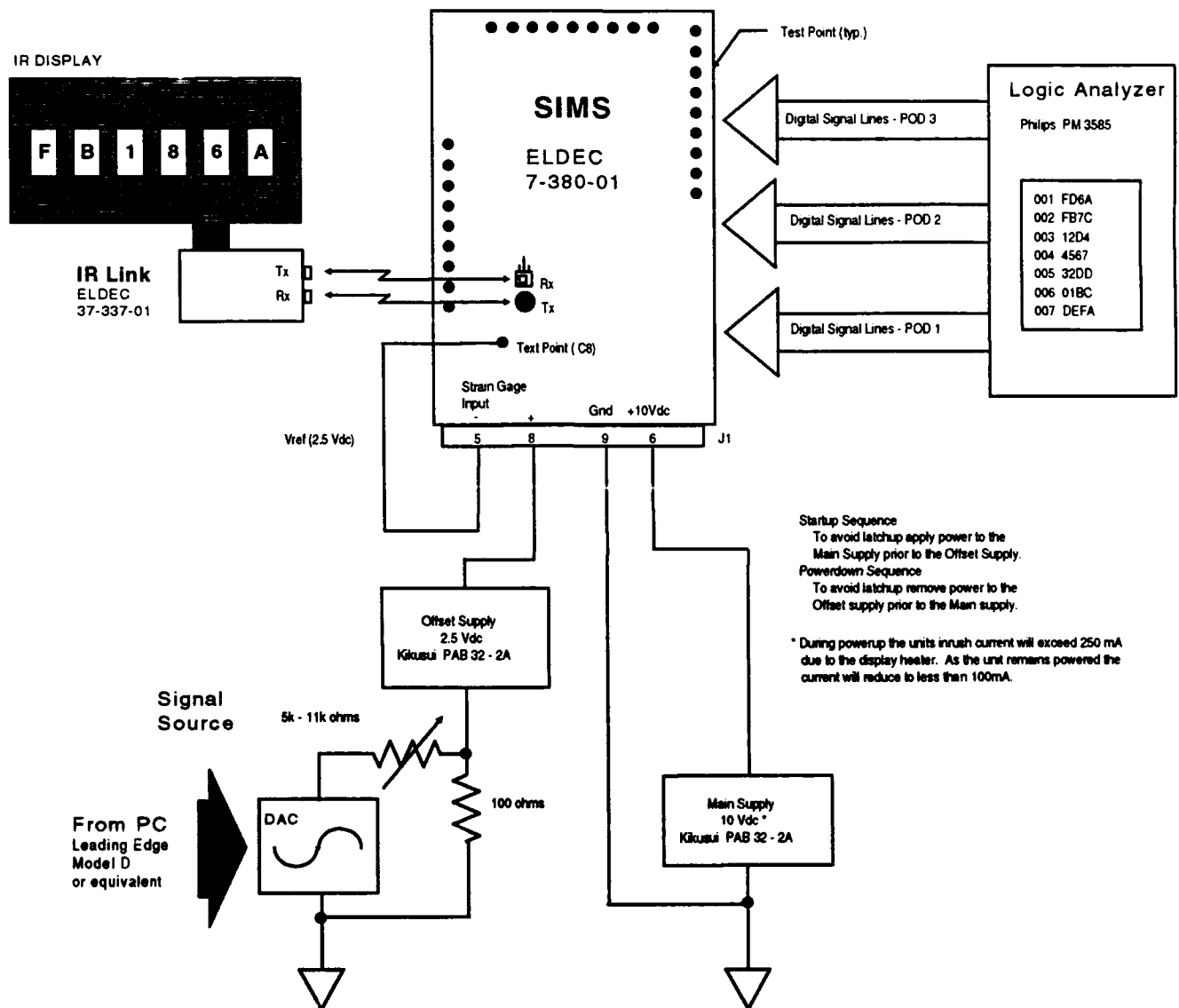


FIGURE 6. TEST SETUP.

2.2.2 Breadboard Tests

The SIMS breadboard was built to verify the functionality of the concept before committing to a printed circuit board design. The breadboard used as much proven "off-the-shelf" electronics as possible, mostly discrete and IC parts.

The input stage was implemented using discrete components, which were later replaced with an ASIC. An Analog-to-Digital converter IC (8-bit) was used to convert the strain gage analog signal to digital form. Most of the Rainflow and Miner's Rule algorithm was first simulated in a digital simulation software package (Viewlogic), then implemented in the FPGAs (Actel). The IR ports (transmit and receive) were built with discrete parts (resistors, capacitors, transistors, LEDs).

The testing process was a series of tests to verify the performance of the critical functions. The key functions considered were the following:

- 1. Input Stage**

The signal conditioning circuit filters and amplifies (20x) the strain gage signal without creating anymore than 20 mv of offset. This makes the calibration of the sensor within an adjustable range. The breadboard verified this function using discrete parts. The ASIC provided even less offset (10 mv).

- 2. Peak Detection/Cycle Count**

The digital logic in the FPGAs track the unclosed cycles and closes the cycle when it receives an equal but opposite unclosed cycle. It also verifies the total cycle count. Using a modulated 200 Hz carrier signal, it was verified that the logic counted the correct number of cycles (30). It also checked the FPGA using the Army data, which was within 5% of actual.

- 3. Power-up/Down**

The power-down circuit stores unclosed cycles in NOVRAM and reloaded the unclosed cycles at power-up. The RAM also stored and refreshed the remaining life count at power-up/down without error. The timing of RAM access was adjusted to make sure the RAM was addressed correctly.

- 4. Curve Fitting Logic**

The curve fitting logic in FPGA simulates the material S-N curve using a piecewise linear approximation of 31 segments scaled to match the actual S-N curve. The linear segments were scaled to match the curve as closely as possible. Each module was programmed to its specific S-N curve.

2.2.3

System Performance Tests

The SIMS module performance tests consisted of two sets, one during the breadboard development phase and the second during the assembly/test of the three deliverable units. The following tests were conducted on the breadboard unit:

1. RAINFLOW LOGIC EVALUATION - this test checked the performance of the logic to detect and count the "UNCLOSED CYCLES" and verify the IR port performance.
2. CONSTANT AMPLITUDE S-N CURVE EVALUATION - this test checked the S-N curve coefficients set in the programmable switches.
3. PEAK DETECTOR PERFORMANCE WITH RANDOM DATA - this test verified the peak detector accuracy against actual data.
4. FATIGUE DAMAGE END-TO-END TEST - this is the final test that verifies the magnitude of the cycles using actual data.

The test performed on the three units is the same as the fatigue damage end-to-end test performed on the breadboard (item 4 above). Test setup and method were similar to the process used for the breadboard tests (see Figure 6). Test data sheets were provided with each unit. The data sheets identify the test by file name. The specific test data was taken from a set of data received from AATD as follows:

AATD Data Description	ELDEC File
Lateral Control Actuator Piston Rod Force (lbs)	Late. dat
Collective Control Actuator Piston Rod Force (lbs)	Coll.dat
Longitudinal Control Actuator Piston Rod Force (lbs)	Long.dat

Test data sheets are provided with each unit.

No environmental tests were performed.

CONCLUSIONS/RECOMMENDATIONS

3.1

CONCLUSIONS

All preliminary testing (ELDEC) has verified that the SIMS concept is feasible and meets the fundamental objective of a small integrated package with real-time fatigue measurement. The data recorded by these tests shows good correlation with the actual field data provided by the Army. However, completion of performance/ environmental testing by AATD is necessary to provide final confirmation of the unit performance/concept. Further development and testing should be continued to arrive at a production configuration for general application.

3.2

RECOMMENDATIONS

Based on the current success of the SIMS development, there are a number of options available depending on applications. To further the application of the SIMS module in real-time fatigue measurement, it is recommended that the module be improved in two general areas:

1. Performance

- Enhance curve fitting algorithm to handle multiple curves easier.
- Provide multi-channel capability through time-multiplexing.
- Integrate all digital logic onto a single gate array.
- Temporarily close out remaining cycles upon IR request for data.
- Develop a better display/ data retrieval system
- Provide a fully battery-operated system

2. Packaging/environment

- Reduce the size by half (3 x 2 x 0.5 inches)
- Support air worthy MIL-SPEC environmental performance

There are also other applications of this concept/ technology such as other sensors (*i.e.*, pressure, temperature).

Any sensor measurement system that entails collection of relative data on a real-time basis at reasonable data rates can be adapted to the SIMS concept. However, specific application will require review of the requirements to determine the degree of applicability/modification.

Some of the advantages of the current SIMS module are: size, real-time, accuracy and low power.

These advantages make the concept a candidate as an element of a data collection/processing system.

RECOMMENDATIONS ON HOW TO IMPLEMENT "FIXES" FOR PERFORMANCE/PACKAGING IMPROVEMENTS

There are eight recommendations to improve the SIMS design. The selection/implementation order of these items is somewhat dependent on the specific requirements for future applications (e.g., flight hardware or lab tests). If lab test/technology improvement is the focus, then the following recommendations on "what", "how" and "when" should be made.

WHAT?

Of the various improvements, the following is the order of importance:

1. Temporarily close out remaining cycles upon IR request for data.
2. Provide a fully battery-operating system.
3. Develop a better display/data retrieval system.
4. Enhance curve-fitting algorithm to handle multiple curves easier.
5. Integrate all digital logic onto a single array.
6. Reduce the size by half (.5 inches).
7. Support airworthy MIL-SPEC environmental performance.
8. Provide multichannel capability through time-multiplexing.

HOW?

The implementation of the improvements falls generally into two categories: hardware and/or programming. Hardware changes involve replacement of components or modification of mechanical subassemblies. Programming changes involve reprogramming the ACTELs or ASIC.

Following are the hardware/programming changes needed to implement the improvements.

1. "Temporarily close out remaining cycles upon IR request for data."

THIS CHANGE REQUIRES REPROGRAMMING OF THE ACTEL CHIPS. NO OTHER CHANGES ARE NECESSARY TO THE MODULE. IT WILL ELIMINATE THE POSSIBILITY OF ERRONEOUS DATA CORRUPTING THE CYCLE COUNT.

2. "Provide a fully battery-operating system."

THIS CHANGE WILL REQUIRE CHANGING THE POWER INPUT DESIGN TO ACCOMMODATE POWER SHUTDOWN TO PRESERVE BATTERY LIFE. IT ALSO REQUIRES A HARDWARE CHANGE TO FIND A SUITABLE MOUNTING LOCATION FOR THE BATTERY.

3. "Develop a better display/data retrieval system."

THIS CHANGE REQUIRES REDESIGN OR REPLACEMENT OF THE IR INPUT/OUTPUT CIRCUITRY. ALSO CONSIDER OTHER MEANS OF GETTING DATA OUT OF THE MODULE (e.g., RS232, FIBER OPTICS). THE DISPLAY NEEDS TO BE REPLACED WITH A MORE ACCURATE AND MORE EFFICIENT MEANS TO READ CUMULATIVE CYCLE DATA.

4. "Enhance curve-fitting algorithm to handle multiple curves easier."

THIS CHANGE REQUIRES REPROGRAMMING OF THE ACTELs TO INCLUDE OTHER S-N CURVES. IT ALSO REQUIRES DEVELOPMENT OF A METHOD OF STORING S-N CURVE DATA AND IMPLEMENTATION THROUGH A LOOKUP TABLE SCHEME.

5. "Integrate all digital logic onto a single array."

THIS CHANGE REQUIRES OPTIMIZATION OF THE ACTEL SOFTWARE AND THE ASIC INTO A SINGLE ARRAY. THIS SHOULD ELIMINATE THE FOUR ACTELs AND ONE ASIC AND REPLACE THEM WITH A SINGLE ARRAY CHIP.

6. "Reduce the size by half (.5 inches)."

THIS CHANGE REQUIRES ITEMS 3 AND 5 BE INCORPORATED BEFORE IT CAN BE IMPLEMENTED. THE SIZE WILL BE DEPENDENT ON WHETHER SOME OF THE OTHER CHANGES ARE IMPLEMENTED (e.g., BATTERY OPERATION).

7. "Support airworthy MIL-SPEC environmental performance."

THIS CHANGE REQUIRES DEFINITION OF AIRWORTHINESS REQUIREMENTS AND REDESIGN FOR BOTH ELECTRONIC COMPONENTS AND STRUCTURE TO COMPLY TO THE AIRWORTHINESS REQUIREMENTS. IT ALSO INVOLVES A SERIES OF VERIFICATION TESTS.

8. "Provide multi-channel capability through time-multiplexing."

THIS CHANGE REQUIRES REDESIGN OF THE COMPLETE MODULE, BOTH HARDWARE AND PROGRAMMING. TO ALLOW FOR MULTICHANNEL OPERATION WILL REQUIRE SOMEWHAT OF A DIFFERENT ARCHITECTURE AND HARDWARE CONFIGURATION.

WHEN?

Implementation of the improvements is dependent on whether they are incorporated individually or together. Individual changes will take less time. The general trend is the highest priority (item 1) is the least time (3 weeks) with the lowest priority (item 8) the longest time (6 months).

**APPENDIX
TEST DATA**

SIMS Proto Board Test Data

Serial No.: Proto 002
 Test Date: 1/10/92
 Material: 7049A

Input Current 95 mA
 Clock Freq. 2.1075 Mhz (R25 = 1.62K)
 MRST Timing 187.4 mS
 ASIC Serial No. 005
 ASIC Offset 7Bh

Waveform Count

		Late.dat		Long.dat		Coll.dat	
		1Run	10 Runs	1Run	10 Runs	1Run	10 Runs
		399	4124	77	910	566	6068
		391	4138	72	910	567	6147
		383	4145	80	896	566	6084
		396	4166	80	969	563	6112
		403	4242	73	973	565	6128
		394	4191	76	973	565	6111
		396	4094	80	975	569	6051
		394	4274	86	921	567	6152
		385	4285	90	977	561	6101
		397	4148	79	973	572	6033
Average =		393.8	418.07	79.3	94.77	566.1	609.87
(Fortran Value)		[413 - 403]		[68 - 71]		[593 - 584]	

Pass/Fail Tests

Pwr Up/Dn Pass
 IR Link Pass
 Final Test _____

SIMS Proto Board Test Data

Serial No.: Proto 003
 Test Date: 1/10/92
 Material: 7049A

Input Current 94 mA
 Clock Freq. 2.087 Mhz (R25 = 1.33K)
 MRST Timing 198.8 mS
 ASIC Serial No. 004
 ASIC Offset 78h

Waveform Count

Late.dat		Long.dat		Coll.dat	
1Run	10 Runs	1Run	10 Runs	1Run	10 Runs
401	4135	81	1019	540	5854
405	4210	72	987	543	5865
397	4230	77	1030	542	5884
404	4126	71	1012	541	5804
385	4178	76	968	540	5842
396	3915	80	1011	540	5889
388	3863	77	1021	528	5846
391	3978	80	988	541	5867
394	3978	77	1023	528	5874
402	3942	79	1035	542	5916
Average =	396.3 405.55	77	100.94	538.5	586.41
(Fortran Value)	[413 - 403]	[68 - 71]		[593 - 584]	

Pass/Fail Tests

Pwr Up/Dn Pass

IR Link Pass

Final Test _____

SIMS Proto Board Test Data

Serial No.: Proto 004
 Test Date: 1/30/92
 Material: 4340 (Steel)

Input Current 94 mA
 Clock Freq. 2.10 Mhz (R25 = 1.33K)
 MRST Timing 191.8 mS
 ASIC Serial No. 007
 ASIC Offset 81h

Waveform Count

Endurance Limit = 0000

	Late.dat		Long.dat		Coll.dat	
	1Run	10 Runs	1Run	10 Runs	1Run	10 Runs
	0	216	0	243	123	1473
	0	216	0	243	123	1473
	0	216	0	243	123	1473
	0	216	0	243	123	1473
	0	216	0	243	123	1473
	0	216	0	243	123	1473
	0	216	0	243	123	1473
	0	216	0	243	123	1473
	0	216	0	243	123	1473
	0	216	0	243	123	1473
Average =	0	21.6	0	24.3	123	147.3

Pass/Fail Tests

Pwr Up/Dn Pass
 IR Link Pass
 Final Test ✓ 80